STUDY OF THE STRUCTURE AND FABRICATION POSSIBILITY OF A NANOSHEET METAL–DIELECTRIC–SEMICONDUCTOR TRANSISTOR ON A GRAPHENE BASE

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Abstract

The rapid evolution of nanoelectronics underscores the need for innovative field-effect transistor (FET) architectures that deliver enhanced performance and enable further miniaturization. This study investigates the design and fabrication potential of a multilayer nanosheet metal-dielectric-semiconductor (MDS) transistor, utilizing semiconducting graphene layers deposited on a silicon substrate and incorporating gold source and drain regions. The graphene layers form contacts with both the upper and lower surfaces of the gold electrodes, resulting in a multilayered gate and channel structure. This configuration allows the gate to fully enclose the channel, thereby improving electrostatic control and optimizing transistor performance parameters. A comprehensive technological modeling process was conducted to define the fabrication sequence, yielding a structure composed of vertically stacked graphene channels encapsulated by silicon dioxide and polycrystalline silicon. Additionally, the study explores a cost-effective and scalable method for depositing graphene layers. This approach involves exfoliating graphite into particles containing varying numbers of graphene layers, which are then dispersed in a liquid medium. Using sharp-edged, blade-shaped probes, these particles are selectively transferred onto the substrate surface, enabling the formation of grapheme layers with controlled thickness and dimensions. The findings demonstrate that the proposed structure and fabrication method can facilitate the development of compact, high-speed MDS transistors, significantly broadening the practical applications of graphene in nano-electronic devices.

Keywords: Graphene, nanoelectronics, field-effect transistor, metal–dielectric–semiconductor, nanosheet structure

1. INTRODUCTION

In the field of nanoelectronics, the ongoing trend of miniaturization has led to performance limitations in conventional MOSFET transistors, particularly concerning channel control, energy efficiency, and integration density. To overcome these challenges, the application of innovative materials and multilayer structures is essential, offering advantages in electrostatic control and high-speed operation. Among the most promising materials are those with two-dimensional (2D) structures, such as transition metal dichalcogenides (TMDs) and graphene, which exhibit exceptional electronic properties and high carrier mobility. TMD materials (e.g., MoS_2, WS_2) feature a tunable bandgap and a high on/off current ratio; however, their carrier mobility and scalability in mass production remain limited [1–3].

Graphene-based field-effect transistors (GFETs) have garnered significant attention in recent years, owing to their high-frequency performance, mechanical flexibility, and compatibility with diverse substrates and fabrication processes.

The performance of GFETs is strongly influenced by the quality of graphene, its interaction with the substrate, and the compatibility of manufacturing processes with CMOS technology [4]. Graphene stands out for its high carrier mobility (>2000 cm²/V·s), high saturation velocity, and thermal stability, making it attractive for high-frequency and analog applications [5]. Bilayer graphene (BLG) is particularly notable for its ability to form a tunable bandgap up to approximately 250 meV under the application of a perpendicular electric field [6].

This study aims to develop an innovative nanosheet MDS transistor structure based on stacked bilayer graphene films. A vertically oriented multilayer channel is proposed to improve gate control and minimize leakage, supported by a scalable and low-cost fabrication method that avoids vacuum-based systems.

The proposed approach includes a double-sided contact configuration between graphene layers and gold electrodes, enabling full channel encapsulation. A selective transfer technique using graphite exfoliation and tip-based probes allows precise control over the width and placement of graphene layers without complex equipment. The fabrication sequence is defined through technological modeling, incorporating silicon dioxide and polycrystalline silicon layers. This study integrates material innovation, structural modeling, and scalable fabrication strategies to advance graphene-based MDS transistors as viable candidates for next-generation nanoelectronics systems.

2. MATERIALS AND METHODS

2.1 Device structure and modeling

Nanosheet MDS transistors, where the channel is fully encapsulated by the gate and dielectric, offer enhanced electrostatic control and reduced leakage currents [7]. Vertical stacking of multiple channels further increases integration density, though fabrication remains technologically challenging. Thus, scalable approaches for multilayer nanosheet transistor fabrication are of high interest. For accurate modeling of nanosheet MDS transistors, the graphene channel regions must be fully encapsulated by subthreshold dielectric and gate materials. Additionally, the structure should allow for the formation of multiple channel regions stacked vertically.

Graphene, as a channel material, provides high carrier mobility, which contributes to achieving a high ON-state current. Under ideal conditions, the high mobility of graphene ($\mu_{ideal} = 2000 \frac{cm^2}{V \cdot s}$) enables maximum current, expressed by the following equation (1).

$$I_{ON,ideal} = \mu_{ideal} \cdot V_g \cdot \frac{W}{L} \cdot k \quad (1)$$

where:

μ_{ideal}- the ideal mobility of graphene ($\frac{cm^2}{V \cdot s}$)

V_g – the gate voltage (V)

W - channel width of the transistor (m)

L – channel length (m)

$k = 0.06 \frac{\mu A}{\mu m \cdot V}$ - is a combined technological coefficient incorporating material and structural parameters [8].

The application of new structures and technological solutions in MDS transistors is driven by the emergence of novel material properties and innovative fabrication approaches.

Table 1 presents the sequential steps for the fabrication of the nanolayer MDS transistor.

Table 1 Sequential teps for the fabrication of the nanolayer MDS transistor

No.	Technological processes	Resulting outcome
1	Thermal oxidation of the surface of a pure silicon substrate, lithography, silicon etching, thermal oxidation	Opening of windows in gate regions, etching, coating with silicon dioxide layer via thermal oxidation
2	Deposition of polycrystalline silicon, surface grinding and polishing, thermal oxidation to form SiO_2	Formation of the first gate and sub-gate dielectric layer
3	Deposition of bilayer graphene and metallic (Au) layers	Formation of semiconducting bilayer graphene and low-ohmic contact with ~2 μm thick gold layer
4	Lithography of the gold layer	Formation of gold source and drain regions
5	Deposition of SiO_2 via PECVD (Plasma Enhanced CVD), deposition of polycrystalline silicon, grinding and polishing	Formation of sub-gate dielectric layer and polycrystalline silicon second gate region
6	Formation of SiO_2 via thermal oxidation, deposition of bilayer graphene, lithography	Formation of low-ohmic contact between graphene and gold, and top bilayer graphene structure
7	Deposition of SiO_2 via PECVD, deposition of polycrystalline silicon, lithography, thermal oxidation of SiO_2 layer	Formation of top sub-gate dielectric and third gate, and protective layer

To minimize device footprint while maximizing current, the nanosheet architecture enables double-sided gating and vertical stacking. In the proposed structure, the channel consists of two semiconducting bilayer graphene sheets, the gate is polycrystalline silicon, the dielectric is SiO_2, and the source/drain are gold, which is shown in **Figure 1**.

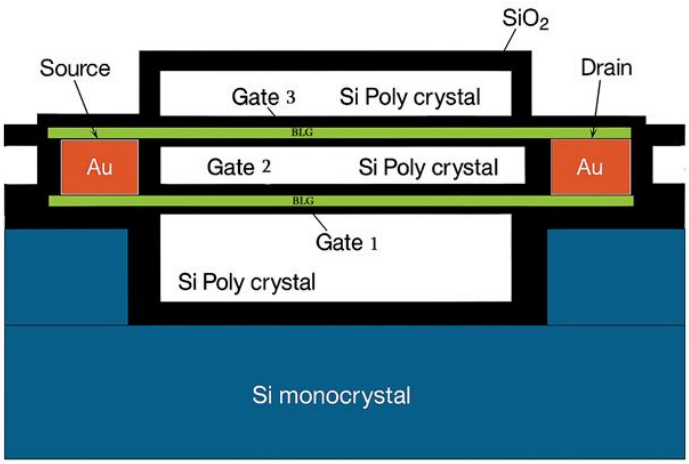

Figure 1 Nanosheet MDS transistor structure

The selection of the subthreshold dielectric is crucial for the device's performance, reliability, and scalability [9-11]. Silicon dioxide (SiO_2) is widely used due to its high technological accessibility, reliable insulation properties, and compatibility with CMOS technology. It provides a smooth and chemically stable interface; however, electrical defects may occur at the Si/SiO_2 interface, which are typically mitigated through passivation and plasma treatment techniques. SiO_2 is selected as the gate dielectric for its technological accessibility, reliable insulation, and CMOS compatibility [12].

2.2 Gate-Induced bandgap engineering in bilayer graphene

Graphene's exceptional electronic, thermal, and mechanical properties have attracted significant scientific interest; however, its lack of an intrinsic bandgap limits its application in electronics and optoelectronics. The

performance of field-effect transistors (FETs) critically depends on the semiconducting nature of the channel, which is defined by the presence of a bandgap. Monolayer graphene (SLG) exhibits high carrier mobility but lacks a bandgap, resulting in low on/off current ratios and high leakage [13].

In contrast, bilayer graphene (BLG) can acquire a tunable bandgap (up to ~250 meV) when subjected to a perpendicular electric field, making it suitable for transistor applications [14]. Experimental studies have demonstrated on/off ratios up to 120 at room temperature with a bandgap of ~170 meV [15]. Graphene also maintains high carrier mobility and is compatible with silicon, even when covered by silicon layers [16].

3. RESULTS AND DISCUSSION

The vertical electric field used in the article is generated by the top and bottom gate electrodes, which are made of polycrystalline silicon and insulated by silicon dioxide (SiO_2). The difference in gate voltages induces displacement fields, D_b and D_t, whose variation ΔD determines the value of the bandgap [17].

The resulting displacement field ΔD between the gates determines the bandgap (Eg) according to equation (2).

$$Eg = \alpha \cdot \Delta D \tag{2}$$

where:

Eg- the bandgap (meV)

α - the proportionality constant $(100meV \cdot \frac{nm}{V})$

ΔD - the average displacement field (V/nm)

The displacement field is calculated as in equation (3):

$$\Delta D = \varepsilon \cdot \frac{Vb - Vt}{d} \tag{3}$$

Where:

ε- the dielectric constant

d - the dielectric thickness (nm)

Vb - the bottom gate voltage (V)

Vt – the top gate voltage (V) [15].

For typical parameter values $\Delta V = 4 \cdot V, \varepsilon = 3.9,\ d = 8\ nm$, the calculated displacement field is as in equation (4).

$$\Delta D = 1.95\ (\frac{V}{nm}) \tag{4}$$

and the corresponding bandgap is as in equation (5).

$$Eg = 195meV \tag{5}$$

In this work, the vertical electric field is applied via top and bottom polycrystalline silicon gates, isolated by SiO_2.

Figure 2 shows the dependence of the bandgap (Eg) on dielectric thickness (d) for different values of ΔV, assuming a constant dielectric constant $\varepsilon = 3.9$. This plot enables the selection of an appropriate ΔV to achieve a desired Eg for a given dielectric thickness.

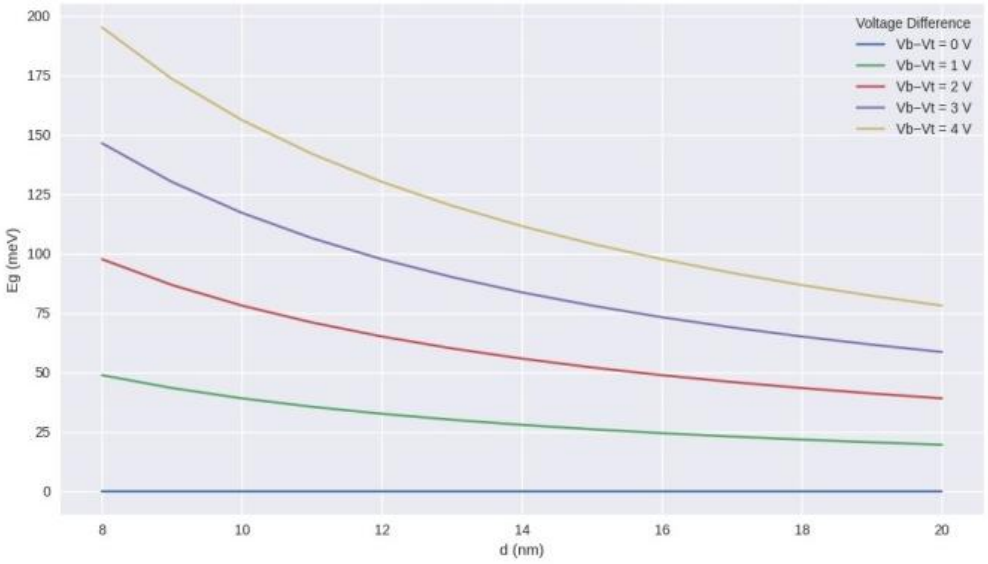

Figure 2 Dependence of the energy bandgap (Eg) on dielectric thickness (d) under varying gate voltages

The tunable bandgap of bilayer graphene (BLG) (~125–190 meV) enables the formation of a semiconducting channel region capable of delivering a high on/off current ratio (~200× at room temperature). This significantly surpasses the performance of single-layer graphene (SLG), which exhibits a much smaller bandgap, and allows BLG to be used in digital and logic circuits without the need for vacuum-grade epitaxial growth. Thus, vertical field-induced bandgap modulation in BLG reduces leakage current and ensures a sharp transition from the off to the on state. This contributes to low-voltage, high-speed transistor operation without additional energy overhead.

Liquid-phase exfoliation (LPE) is an efficient method for obtaining high-yield graphene dispersions. The process involves intercalation, ultrasonic exfoliation, and centrifugation to separate flakes by thickness [18] :

In this work, high-purity graphite (Sigma-Aldrich, ≥99.9%) was ball-milled, dispersed in Cyrene (~1.5 mg/mL), sonicated (20 kHz, 60 min, ice bath), and centrifuged at 4000 rpm for 30 min. Mono- and bilayer graphene flakes were collected from the upper fraction.

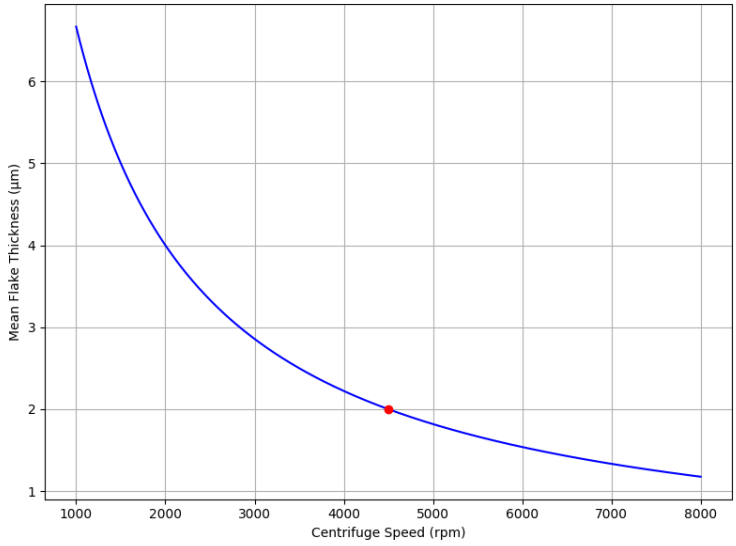

Figure 3 Dependence of the average thickness (number of layers) of graphene flakes on centrifugation speed

Figure 3 shows the dependence of the average thickness (number of layers) of graphene flakes on centrifugation speed. According to the graph, BLG is obtained at speeds above ~4000 rpm.

It should be emphasized that the choice of solvent plays a critical role and must ensure efficient transfer of exfoliation energy, minimal energy required to break van der Waals interactions, and stabilization to prevent re-aggregation of flakes [19]. The dynamic viscosity of the solvent is also a critical parameter in terms of exfoliation efficiency and dispersion stability. High viscosity can promote the production of high-yield, low-defect graphene; however, excessive viscosity may hinder the separation of thin and lightweight flakes during the centrifugation stage [20]. In this study, Cyrene was selected as the exfoliation solvent due to its optimal viscosity, high polarity, and excellent dispersion stability. Cyrene enables efficient energy transfer during sonication and prevents re-aggregation of exfoliated flakes, making it particularly suitable for isolating bilayer graphene (BLG) with minimal defects and controlled thickness. **Figure 4** shows graphene layer formation on Si/SiO_2 substrates via nanolithographic method.

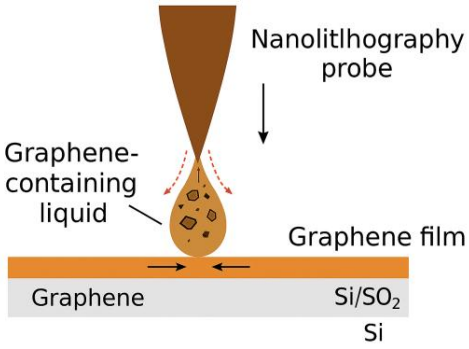

Figure 4 Graphene layer formation on Si/SiO_2 substrates via nanolithographic method

Bilayer graphene (BLG) samples were deposited onto Si/SiO_2 substrates using feather nanolithography. A sharp probe delivered the graphene-containing liquid at a controlled rate (100 nm/s) while maintaining a 5 nm gap between the probe and substrate, resulting in uniform, continuous graphene films. The process parameters, flake concentration, probe substrate distance, movement speed, substrate temperature, and solvent type were optimized to minimize voids and ensure film uniformity. After initial separation, the thinnest flake-containing solution was further refined and applied to the substrate using the same method, enabling precise control over the number of graphene layers.

4. CONCLUSION

This study introduces an innovative nanosheet MDS transistor architecture utilizing bilayer graphene (BLG) as the semiconducting channel material. The proposed design demonstrates significant improvements in electrostatic control, leakage current suppression, and structural scalability key parameters for advancing future nano-electronic systems. By employing a vertically stacked channel configuration with polycrystalline silicon gate electrodes and silicon dioxide (SiO_2) dielectrics, the architecture achieves compact integration while maintaining high performance. A notable contribution of this work is the fabrication methodology, which combines liquid-phase exfoliation with selective layer transfer using nano lithographic probes. This approach enables precise control over graphene layer thickness and uniformity without relying on vacuum-based epitaxial growth, thereby enhancing manufacturability and reducing process complexity. The ability to isolate and integrate bilayer graphene flakes with tunable bandgap properties allows for sharp on/off switching behavior and low-voltage operation, making the device highly suitable for digital and logic applications. Overall, the integration of semiconducting BLG into nanosheet MDS transistors represents a promising pathway toward the development of energy-efficient, high-speed, and scalable nano-electronic devices. The results of this

research lay the groundwork for future exploration of multilayer graphene systems and their potential in next-generation transistor technologies.

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